CLAIMS:

1. A method of forming a pattern of features having sub-micron width in a device substrate layer, which method includes the steps of

forming a resist layer of one the resist types: positive resist and negative resist on the substrate;

providing a mask having a mask pattern corresponding to the pattern of features to be formed in the substrate layer;

illuminating the resist layer via the mask pattern by means of a projection beam providing an exposure dose, thereby generating an acid concentration profile in the resist layer around each imaged feature;

heating the illuminated resist layer during a post exposure baking (PEB) step so that, starting from the highest illumination intensity areas the material of a positive resist layer becomes soluble and the material of a negative resist layer becomes insoluble, respectively in a developer solution;

developing the resist layer in the developer solution so that resist material is removed from resist layer areas having a solubility above a threshold value so that a resist profile pattern is obtained;

removing material from or adding material to areas of the substrate layer, which areas are delineated by the resist profile pattern, so that the required pattern of features is formed in the substrate layer, characterized in that the time duration of the PEB step and the exposure dose are adapted to the design width of the features to be formed.

2. A method as claimed in claim 1, wherein during the PEB step transitions between non-soluble and soluble resist material initially have a negative slope, characterized in that an enlarged PEB time duration is used to push the slopes to at least zero slopes and preferably positive slopes.

3. A method as claimed in claim 1 or 2, characterized in that a resist layer having a thickness in the range of 300 to 350 nm is used.

4. A method as claimed in claim 1 or 3, characterized in that a resist having an adapted radiation absorption gradient is used to reduce changes in the slopes of transitions between non-soluble and soluble resist material which are due to extended PEB time duration.

5. A method as claimed in claims1, 2, 3 or 4 using a same mask pattern for successively forming a same pattern in a substrate layer of a batch of substrates by means of a same lithographic exposure apparatus, characterized in that for carrying out the PEB steps for successively exposed substrates a number of PEB devices is used, which number substantially corresponds to the ratio of the PEB time duration and the exposure time for one substrate.

6. A method as claimed in any one of claims 1 to 5, wherein the step of providing a mask pattern includes designing a pattern having optical proximity correction features, characterized in that in the design stage the envisaged PEB time duration is used as a design parameter to determine the design width of the design pattern of features.

7. A method as claimed in any one of claims 1-6, characterized in that the time duration of the PEB step is enlarged to form device features having a smallest dimension, which is smaller than the corresponding dimension in an aerial image of the mask pattern, the aerial image being formed by the projection beam in the resist layer.

8. A method as claimed in claim 7, characterized in that the PEB step is performed during at least 140 seconds and that a correspondingly smaller exposure dose is used to obtain feature widths smaller than 80 nm.

9. A method as claimed in any one of claims 1 to 6, for use in a lithographic process having an isofocal CD, characterized in that the isofocal CD is tuned to the design CD by adapting the PEB time duration and the exposure dose.

10. A method as claimed in any one of claims 1 to 9, characterized in that use is made of a binary mask pattern.

11. A method as claimed in any one of claims 1 to 9, characterized in that use is made of a phase shifting mask pattern.

12. A method of level-by-level manufacturing of a device, which comprises device features distributed over different levels, which method employs a number of processes for configuring device features each process for one device level, characterized in that at least one of the configuring processes comprises the method as claimed in any one of claims 1-11.

13. A device manufactured by means of the method as claimed in any one of claims 1-12.